CLAIMS:

1. An integrated circuit (40) comprising a plurality of computation islands (30), each computation island (30), each computation island (30) operating at one or more utility values, at least one utility value of a first computation island being different from a corresponding utility value of a second computation island, the integrated circuit (40) being provided with monitoring means (43) for monitoring at least one working parameter related to a working condition of the integrated circuit (40), and at least two computation islands being provided with a local control device (36) for independently tuning at least one utility value for at least one computation island, based on the monitored at least one working parameter, wherein the local control devices (36) are provided with communication means to communicate with a global controller (42) so as to obtain a pre-set level of performance of the integrated circuit (40).

2. An integrated circuit (40) according to claim 1, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck).

3. An integrated circuit (40) according to claim 2, wherein the transistor threshold voltage is determined by a bulk voltage of some transistors in a computational island (30).

4. An integrated circuit (40) according to claim 1, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, clock frequency value.

5. An integrated circuit (40) according to claim 1, wherein the pre-set level of performance relates to any or all of power consumption or speed of the integrated circuit (40).

6. An integrated circuit (40) according to claim 1, wherein each computation island (30) is placed in an isolated third well of a triple-well CMOS technology.

7. An integrated circuit (40) according to claim 1, furthermore comprising at least one interface island (39) for interfacing among computation islands (30).

8. An integrated circuit (40) according to claim 7, wherein at least two interface islands (39) are placed in a common third well, or substrate, of a triple-well CMOS technology.

9. An integrated circuit (40) according to claim 1, a computation island (30) furthermore comprising an actuator (34) for tuning a utility value in a monitored utility value-regulating closed-loop system.

10. An integrated circuit (40) according to claim 1, a computation island (30) furthermore comprising a local monitoring means (38) for monitoring local working parameters of the computation island (30).

11. A method for real-time tuning of at least one utility value of an integrated circuit (40) comprising a plurality of computation islands (30), each computation island (30) operating at one or more utility values, at least one utility value of a first computation island being different from a corresponding utility value of a second computation island, at least two computation islands being provided with a local control device (36) for independently tuning at least one utility value for at least one computation island (30), the method comprising

- monitoring of at least one working parameter related to a working condition of the integrated circuit (40),
- based on the monitored at least one working parameter, independently tuning at least one utility value for at least one computation island (30) by means of its local controller (36), and
- controlling the local controllers (36) of the computation islands (30) by means of a global controller (42) so as to obtain a pre-set level of performance of the integrated circuit (40).

12. A method according to claim 11, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck).

13. A method according to claim 11, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, clock frequency value.

14. A method according to claim 11, wherein the pre-set level of performance relates to any or all of power consumption or speed of the integrated circuit (40).

15. A method according to claim 11, wherein the integrated circuit (40) is designed based on utility values different from their nominal values.